REMARKS

The Office Action mailed on February 4, 2003, has been received and reviewed.

Claims 1-79 were previously pending in the above-referenced application. Claims 1-16, 20-57, 60-77, and 79 stand rejected. Claims 17-19, 58, 59, and 78 have been objected to as being dependent upon rejected base claims, but the indication that each of these claims recites allowable subject matter is noted with appreciation. Claims 15, 36, 57, and 77 have been canceled without prejudice or disclaimer. New claims 80-118 have been added.

Reconsideration of the above-referenced application is respectfully requested.

Information Disclosure Statement

Please note that an Information Disclosure Statement was filed in the above-referenced application on February 18, 2003. It is respectfully requested that the references cited in the Information Disclosure Statement and listed on its accompanying Form PTO/SB/08 be considered and made of record in the above-referenced application and that an initialed copy of the Form PTO/SB/08 evidencing such consideration be returned to the undersigned attorney.

Drawings

Corrections to the drawings are respectfully submitted herewith, under cover of a separate Letter to the Chief Draftsman. All corrections have been marked in red. Approval of the corrections to the drawings is respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

Claims 21, 22, 26, 28, 33-41, 45-48, 51-57, 60-66, 70, 71, 73-77, and 79 stand rejected under 35 U.S.C. § 102(e) as being anticipated by the disclosure of U.S. Patent 6,476,507 to Takehara (hereinafter "Takehara").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference that qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Furthermore, the identical invention must be shown in as complete detail as is

contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Additionally, the elements must be arranged as required by the claim, but identity of the terminology is not required. *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990).

Takehara describes a semiconductor device assembly that includes a semiconductor die, a tape positioned over and secured to an active surface of the semiconductor die, and a substrate element positioned over and secured to the tape. The semiconductor die includes bond pads that are arranged substantially linearly. The tape includes a slot through which the bond pads of the semiconductor die are exposed. Takehara also explains, at col. 11, lines 43-45, that the slot may extend beyond the outer periphery of the semiconductor die. The substrate includes a slot which is aligned with the slot of the tape.

When the assembly of Takehara is packaged, it is introduced into a cavity 13, 14 of a mold 10, 11. Col. 7, lines 54-65. As is well known in the art, although the assembly will be held in place within the mold cavity 13, 14, the mold is not actually secured to the substrate but, rather, may be biased thereagainst.

Independent claim 21, as amended and presented herein, recites a semiconductor device assembly which includes, among other things, a semiconductor die, a tape, and a substrate element. The semiconductor device assembly of amended independent claim 21 also comprises a coverlay. The coverlay is secured to an opposite surface of said substrate element from that which is secured to the tape. Additionally, the coverlay substantially covers at least one opening formed through the substrate element.

By way of contrast with amended independent claim 1, Takehara lacks any express or inherent description of a semiconductor device assembly that includes a coverlay that substantially covers at least one opening formed through a substrate element. As noted previously herein, the upper mold 10 described in Takehara does not comprise a coverlay. Nor is the upper mold 10 described in Takehara secured to a surface of the substrate element of the semiconductor device assembly described therein.

Accordingly, it is respectfully submitted that Takehara does not anticipate each and every element of amended independent claim 21, as is required to maintain a rejection under

35 U.S.C. § 102(e). Thus, under 35 U.S.C. § 102(e), amended independent claim 21 is allowable over Takehara.

Claims 22, 26, 28, 33-35, and 37-40 are each allowable, among other reasons, as depending either directly or indirectly from claim 21, which is allowable.

Claim 36 has been canceled without prejudice or disclaimer, rendering the rejection thereof moot.

Independent claim 41, as amended and presented herein, recites a method for packaging at least an active surface of a semiconductor die. The method of independent claim 41 includes positioning a tape over an active surface of a semiconductor die, positioning a substrate element over the tape, electrically connecting at least one bond pad of the semiconductor die to at least one contact pad of the substrate element, and securing a coverlay to an exposed surface of the substrate element. The coverlay is positioned so as to substantially cover at least one opening formed through the substrate element. Enclapsulant material is then introduced into a receptacle formed by the coverlay, openings through the tape and the substrate element, and the semiconductor die.

It is respectfully submitted that Takehara does not expressly or inherently describe that a coverlay is positioned over an exposed surface of a substrate element. Rather, the description of Takehara is limited to positioning an upper mold 10 over the substrate element of the semiconductor device assembly described therein.

Further, it is respectfully submitted that the mold 10 of Takehara is not secured to the exposed surface of the substrate element of the semiconductor device assembly described in Takehara. Rather, the upper mold 10 is merely biased against the exposed surface of the substrate element.

For these reasons, it is respectfully submitted that Takehara does not anticipate each and every element of amended independent claim 41. It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), amended independent claim 41 is allowable over Takehara.

Each of claims 45-48, 51-56, and 60-62 is allowable, among other reasons, as depending either directly or indirectly from claim 41, which is allowable.

Claim 57 has been canceled without prejudice or disclaimer, rendering the rejection thereof moot.

Independent claim 63 recites a method for preparing a semiconductor die for packaging. That method includes, among other things, positioning a tape over an active surface of a semiconductor die, positioning a substrate element over the tape, electrically connecting at least one bond pad of the semiconductor die to at least one contact pad of the substrate element, and securing a coverlay to the substrate element. The coverlay is positioned so as to substantially cover at least one opening formed through the substrate element.

Again, Takehara includes no express or inherent description of positioning a coverlay over a substrate. Instead, the description of Takehara is limited to positioning a semiconductor device assembly within a mold cavity 13, 14, with an upper mold 10 half being positioned adjacent to a substrate of the assembly.

Moreover, Takehara neither expressly nor inherently describes that the upper mold 10 is secured to the substrate. Rather, as is well known in the art, the upper mold half would merely be biased against the substrate.

Therefore, it is respectfully submitted that Takehara does not anticipate each and every element of amended independent claim 63. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(e), amended independent claim 63, is allowable over Takehara.

Claims 64-66, 70, 71, 73-76, and 79 are each allowable, among other reasons, as depending either directly or indirectly from claim 63, which is allowable.

As claim 77 has been cancelled without prejudice or disclaimer, it is respectfully submitted that the rejection thereof is moot.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 21, 22, 26, 28, 33-41, 45-48, 51-57, 60-66, 70, 71, 73-77, and 79 be withdrawn.

Rejections Under 35 U.S.C. § 102(e)/ 35 U.S.C. § 103(a) Obviousness Rejections

Takehara or, in the Alternative, Takehara in View of Sasaki

Claims 1, 2, 6, 7, 9, 10, 15, 16 and 20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Takehara or, in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Takehara in view of U.S. Patent 6,175,159 to Sasaki (hereinafter "Sasaki").

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Independent claim 1, as amended and presented herein, recites a semiconductor device assembly that includes, among other things, a semiconductor die, a tape, and a substrate element. The semiconductor device assembly of amended independent claim 1 also comprises a coverlay. The coverlay is secured to an opposite surface of said substrate element from that which is secured to the tape. Additionally, the coverlay substantially covers at least one opening formed through the substrate element.

Neither Takehara nor Sasaki describes, teaches, or suggests a semiconductor device assembly that includes a coverlay that is positioned over a surface of a substrate element of the assembly.

Further, Takehara and Sasaki both lack any teaching or suggestion that a coverlay may be secured to a surface of a substrate element of a semiconductor device assembly, as recited in amended independent claim 1.

It is, therefore, respectfully submitted that Takehara does not anticipate each and every element of amended independent claim 1. It is also submitted that Takahara and Sasaki do not render amended independent claim 1 obvious or unpatentable. Accordingly, it is respectfully

submitted that, under 35 U.S.C. § 102(e), amended independent claim 1 is allowable over Takehara and that, under 35 U.S.C. § 103(a), amended independent claim 1 is allowable over both Takehara and Sasaki, taken either separately or together.

Claims 2, 6, 7, 9, 10, 16 and 20 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 15 has been cancelled without prejudice or disclaimer, rendering the rejection thereof moot.

Takehara or, in the Alternative, Takehara in View of Sasaki

Claims 5, 25, 27, and 69 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takehara or, in the alternative, over Takehara in view of Sasaki.

Claim 5 is allowable, among other reasons, as depending from claim 1, which is allowable.

Claims 25 and 27 are both allowable, among other reasons, as respectively depending directly and indirectly from claim 21, which is allowable.

Claim 69 is allowable, among other reasons, as depending from claim 63, which is allowable.

Takehara or, in the Alternative, Takehara in View of Sasaki, Toh and Farnworth

Claims 8 and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takehara or, in the alternative, over Takehara in view of Sasaki and, further, in view of U.S. Patent 6,091,140 to Toh et al. (hereinafter "Toh") and U.S. Patent 6,020,629 to Farnworth et al. (hereinafter "Farnworth").

Claim 8 is allowable, among other reasons, as depending from claim 1, which is allowable.

Claim 44 is allowable, among other reasons, as depending indirectly from claim 41, which is allowable.

Takehara in View of Eng or, in the Alternative, Takehara in View of Sasaki and Eng

Claims 3, 4, 11-14, 23, 24, 29-32, 42, 43, 49, 50, 67, 68, and 72 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takehara in view of U.S. Patent 6,087,203 to Eng et al. (hereinafter "Eng") or, in the alternative, Takehara in view of Sasaki and, further, in view of Eng.

Each of claims 3, 4, and 11-14 is allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claims 23, 24, and 29-32 are each allowable, among other reasons, as depending either directly or indirectly from claim 21, which is allowable.

Each of claims 42, 43, 49, and 50 is allowable, among other reasons, as depending either directly or indirectly from claim 41, which is allowable.

Claims 67, 68, and 72 are each allowable, among other reasons, as depending either directly or indirectly from claim 63, which is allowable.

Allowable Subject Matter/New Claims

The indication that claims 17-19, 58, 59, and 78 recite allowable subject matter is gratefully acknowledged.

New independent claim 80 has been added to recite the subject matter that appears in claim 19 and the claims from which it depends. New claims 81-99 depend from new independent claim 80 and recite substantially the same subject matter as that recited in claims 2-13, 15 (which has been canceled), 14, 16-18, and 20, respectively.

New independent claim 99 is a method claim which includes limitations similar to those of claims 19 and 63. New claims 100-115 depend from new independent claim 99 and recite substantially the same subject matter as that recited in claims 64-76, 77 (which has been canceled), 78, and 79, respectively.

It respectfully submitted that, in view of the remarks that are provided in the outstanding office action with respect to the allowability of the subject matter recited in claim 19, that new independent claims 80 and 99 are both allowable, as are each of the claims that depend therefrom.

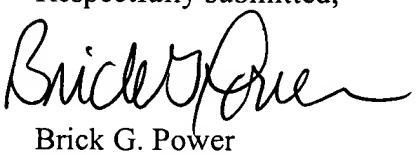
New claims 116-118 depend from claim 24 and recite subject matter similar to that recited in claims 17 and 18.

It is respectfully submitted that none of new claims 80-118 introduces new matter into the above-referenced application.

CONCLUSION

It is respectfully submitted that each of claims 1-14, 16-35, 37-56, 58-76, and 78-118 are allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

1. (Twice amended) A semiconductor device package, comprising:

a semiconductor die with a plurality of bond pads arranged on an active surface thereof;

a tape positioned over said active surface, said tape including at least one slot formed therethrough, each of said plurality of bond pads being exposed through said at least one slot, at least one end of said at least one slot extending beyond an outer periphery of said semiconductor die;

a substrate element positioned over said tape opposite said semiconductor die, said substrate element including a plurality of contact areas, each contact area of said plurality corresponding to a bond pad of said plurality of bond pads and electrically connected thereto by way of an intermediate conductive element that extends through at least one opening formed through said substrate element and aligned with said at least one slot of said tape, said substrate element further including a contact pad in communication with each contact area of said plurality of contact areas by way of a substantially laterally extending conductive trace; [and]

a quantity of encapsulant material substantially filling a volume defined by said at least one slot of said tape and said at least one opening of said substrate element; and

a coverlay secured to a surface of said substrate element opposite said tape, said coverlay substantially covering at least said at least one opening through said substrate element.

16. (Amended) The semiconductor device package of claim [15] 1, wherein said coverlay comprises a recessed area within which each intermediate conductive element is contained.

17. (Amended) The semiconductor device package of claim [15] 1, wherein said coverlay is secured to said substrate element with an adhesive material.

19. (Amended) The semiconductor device package of claim [15] 1, wherein contact pads of said substrate element are exposed through or beyond said coverlay.

21. (Amended) A semiconductor device assembly, comprising:

a semiconductor die with at least one bond pad on an active surface thereof;

a tape secured to said active surface, said tape including a slot formed therethrough with said at least one bond pad being exposed through said slot, at least one end of said slot extending beyond an outer periphery of said semiconductor die; [and]

a substrate element positioned over said semiconductor die opposite said tape from said semiconductor die, said substrate element including at least one opening formed therethrough through which said at least one bond pad is exposed; and

a coverlay secured to a surface of said substrate element opposite said tape, said coverlay substantially covering at least said at least one opening through said substrate element.

37. (Amended) The assembly of claim [36] 21, wherein said coverlay includes a recessed area configured to communicate with said at least one opening.

39. (Amended) The assembly of claim [36] 21, wherein said coverlay, said at least one opening formed through said substrate element, said slot formed through said tape, and said semiconductor die together form a receptacle.

41. (Twice amended) A method for packaging at least an active surface of a semiconductor die, comprising:

positioning a tape over the active surface so that at least one bond pad on the active surface is exposed through a slot formed through said tape and at least one end of said slot extends beyond an outer periphery of the semiconductor die;

positioning a substrate element over said tape so that said at least one bond pad is exposed through at least one opening formed through said substrate element and aligned with said

slot, said substrate element including at least one contact area corresponding to said at least one bond pad;

electrically connecting said at least one bond pad to said at least one contact area;

[positioning] securing a coverlay [on] to an exposed surface of said substrate element to substantially cover said at least one opening formed through said substrate element; and

introducing encapsulant material through said at least one end into a receptacle formed by said coverlay, said at least one opening, said slot, and said semiconductor die from a location opposite the semiconductor die from said tape.

58. (Amended) The method of claim [57] 41, wherein said securing comprises securing said coverlay to said substrate element with a pressure sensitive adhesive.

63. (Amended) A method for preparing a semiconductor die for packaging, comprising:

positioning a tape over at least an active surface of the semiconductor die, said tape including a slot through which at least one bond pad on the active surface of the semiconductor die is exposed, at least a portion of said slot extending laterally beyond an outer periphery of the semiconductor die;

positioning a substrate element over said tape with at least one opening formed through said substrate element being located at least partially over said slot; and

[positioning] securing a coverlay [over] to said substrate element to substantially seal said at least one opening, said coverlay and lateral edges of said at least one opening and said slot forming a receptacle.

78. (Twice amended) The method of claim [77] 63, wherein said securing comprises adhesively securing said coverlay to said substrate element.

79. (Amended) The method of claim [77] 63, wherein said securing comprises removably securing said coverlay to said substrate element.